Scaling Metal Silicide Contacts in Microelectronics: At What Size Will Microstructure Affect Electrical Properties?

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With the continued scaling of CMOS technology, the typical contact area to the source and drain of a CMOS device can now reach below 1000 nm^2. At these nano-dimensions, typical intrinsic contact resistivities of $1x10^{-8}$ □□cm^2 easily lead to resistances exceeding the k□ solely for crossing the silicide-silicon interface. Such resistances are unacceptable as they dominate the overall resistance of a device. In an attempt to mitigate this increase in interfacial resistance with contact area reduction, much research has been performed concentrating on the tailoring of material properties of both the silicide and the semiconductor substrate as well as on the optimization of contact geometries and the advanced engineering of interfaces.

As the size of the contact reaches dimensions that are similar or smaller than the typical microstructure of the expected poly crystalline material, some dramatic effects are to be anticipated. First, the presence of a single grain during the silicidation eliminates the typical dominant diffusion path: grain boundaries. As a result, phase nucleation and kinetics of growth can only proceed through the silicide bulk or the available interfaces. This will likely retard formation of the desired phases in the narrowest dimensions. Another expected disadvantage of very small contacts resides in the variability of the intrinsic contact resistance discussed above. It is accepted that the Schottky barrier height of a given silicide to a silicon substrate varies with substrate orientation. As a result, variation of crystal orientation from contact to contact may lead to dramatic effects on contact resistance. This orientation variation can originate from either a variation in silicide texture from contact to contact or a variation in device geometry (i.e. silicidation on Si(100), Si(110) or Si nanowire device depending on geometry).

In this presentation, we will explain how the contact resistivity is expected to become a major limiter of device performance and describe some of the challenges involved in making relevant nanostructures and characterizing them. As devices are now built on pitches which are smaller than 100 nm, the need for more efficient/ better characterization tools will be discussed.